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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,624	07/15/2003	Noboru Matsuda	240349US2TTCCONT	5650

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EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,624	MATSUDA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/15/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 13 and 19 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 13 and 19 repeat the subject matter of independent claim 11, they fail to further limit the subject matter of independent claim 11.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (US. 4,663,644).

Regarding claim 1, Shimizu (Figs. 1 and 3E) discloses a semiconductor device comprising: a first electrode gate group 4 having a plurality of gate electrodes 4a formed on a semiconductor substrate 6 to be away from each other at first equal spacing 5; source contact 12 having a portion 13 formed separated from a first gate electrode 4a of the first electrode gate group 4 by a second spacing (see Fig. 3E, second spacing equals the sum of first spacing 5 and a spacing portion of layer 8) greater than the first

spacing 5; and source regions 9 for electrically interconnecting the first gate electrode group 4 and the source contact 12.

Regarding claims 2-3, as discussed above, Shimizu (Figs. 1 and 3E) discloses he invention as claimed, including the source regions 9 are electrically connected to each other at one end of the first gate electrode group (right hand end) by the source contact 12 and separated from each other at the other end of the first gate electrode (left hand end).

Regarding claim 4, Shimizu (Figs. 1 and 3E) discloses a semiconductor device comprising: a first gate electrode group 4 having a plurality of gate electrodes 4a formed on a semiconductor substrate 6 to be away from each other at the first equal spacing 5; a second gate electrode group 4 having a plurality of gate electrodes 4a formed on the semiconductor substrate 6 to be away from each other at the first equal spacing 5; a source contact portion 13 between the first and second gate electrode groups 4 to be away from the first and second gate electrode groups 4 at a second spacing; and source regions 9 for electrically interconnecting the first gate electrode group 4 and the source contact 13, wherein the source regions 9 are electrically connected to each other at one end of the first gate electrode group 4 (right hand end) by the source contact 12, and separated from each other at the other end of the first gate electrode group 4 (left hand end).

Regarding claims 5-8, Shimizu (Figs. 1 and 3E) further discloses that the gate electrodes 4a of the first group 4 are connected to each other at the other end (not shown in Fig. 1, see Fig. 2), the first and second gate electrode groups 4 are formed in

trench structures, and the diffused source regions 9, the source contact 12 and the first gate electrode group 4 constitute one MOS transistor.

Regarding claims 9-10, Shimizu (Fig. 1) also discloses a source electrode 12 on the semiconductor substrate, wherein the source contact portion 13 is an electrode drawn from the source electrode 12, and all the gate electrodes 4a of the first gate electrode group 4 are used as gates for a MOS transistor.

Regarding claims 11, 13 and 19, Shimizu (Figs. 1 and 3E) discloses a semiconductor device comprising: a first gate electrode group 4 (the rightmost group) having a plurality of gate electrodes 4a formed on a semiconductor substrate 6 to be away from each other at first equal spacing; a second gate electrode group 4 (the second rightmost group) having a plurality of gate electrodes 4a on the semiconductor substrate 6 to be away from each other at the first equal spacing 5; a third gate electrode group 4 (the third rightmost group) having a plurality of gate electrodes 4a formed on the substrate 6 to be away from each other at the first equal spacing 5; a first source contact portion 13 formed between the first and second gate electrode groups 4 to be away from the first and second gate electrode groups 4 at a second spacing; a second source contact portion 13 formed between the second and third gate electrode groups 4 to be away from one selected from the second and third gate electrode groups 4 at the second spacing; first source regions 9 which electrically interconnect the first gate electrode group 4 and the first source contact portion 13; and second source regions 9 which electrically interconnect the second gate electrode group 4 and the second source contact portion 13, wherein the first source regions 9 are electrically

connected to each other at one end of the first gate electrode group 4 (right hand end) by the source contact electrode 12 and separated from each other at the other end of the first gate electrode group (left hand end), and the second source regions 9 are electrically connected to each other at one end of the second gate electrode group 4 (right hand end) by the source contact electrode 12 and separated from each other at the other end of the second gate electrode group (left hand end).

Regarding claims 12, 14, 15 and 16, Shimizu (Figs. 1 and 3E) further discloses that: the first and second gate electrode groups 4 are connected to each other at the other end (not shown in Fig. 1, see Fig. 2); the first and second gate electrode groups 4 are formed in trench structures; the diffused first source region 9, the first source contact portion 13, and the first gate electrode group 4 constitute one MOS transistor; and the diffused second source region 9, the second source contact portion 13, and the second gate electrode group 4 constitute another MOS transistor.

Regarding claims 17 and 18, Shimizu (Figs. 1 and 3E) further disclose that each of the first and second source contact portions 13 is an electrode drawn from a source electrode 12, and these portions are connected to each other (see Fig. 3E), and all the gate electrodes 4a of the first and second gate electrode groups 4 are used as gates for MOS transistors.

Regarding claim 20, Shimizu (Fig. 3E) also discloses that the second spacing (second spacing equals the sum of the first spacing 5 and a spacing portion of layer 8) is greater than the first spacing 5.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
February 4, 2005

PHAT X. CAO
PRIMARY EXAMINER